

What is claimed is:

1. A magneto-resistive memory array, comprising:
 - an array of magneto-resistive memory cells, the memory cells forming a plurality of rows and a plurality of columns;
 - a plurality of sense lines having first and second ends, each sense line interconnecting a plurality of memory cells in a selected one of the rows in the plurality of rows of the array and providing a sense point located between the first and second ends of the sense line;
 - a plurality of word lines, each word line passing adjacent to two, complementary memory cells in each row of the plurality of rows of the array; and
 - a plurality of serpentine bit lines, each serpentine bit line disposed adjacent to the memory cells in one row of the array such that current flowing in the serpentine bit line passes in first and second, different directions for adjacent memory cells in the row.
2. The memory array of claim 1, wherein each sense line provides a voltage output at a midpoint of the sense line.
3. The memory array of claim 2, wherein each word line passes adjacent to the array of memory cells in a substantially U-shaped path.
4. The memory array of claim 2, wherein one memory cell of the two, complementary memory cells in a row associated with a common word line is located on a first side of the midpoint of the sense line and the other memory cell is located on the other side of the midpoint of the sense line.
5. The memory array of claim 1, wherein each serpentine bit line comprises:
 - a plurality of first portions, the first portions extending parallel to the row of memory cells of the array;
 - a plurality of second portions, each second portion disposed adjacent to one of the memory cells in the associated row of the array; and
 - wherein each second portion is coupled to adjacent first portions such that

current in the serpentine bit line flows in substantially opposite directions for adjacent memory cells in the row of the array.

6. The memory array of claim 1, and further including a sense circuit, the sense circuit comprising:

a sample and hold circuit adapted to sample and hold a voltage from one of the plurality of sense lines; and

a comparator, coupled to the one of the plurality of sense lines and the sample and hold circuit, the comparator adapted to determine the data stored in the complementary memory cells based on the sampled voltage and the voltage of the sense line.

7. A method for reading a value from a magneto-resistive memory device, the method comprising:

reading a first voltage at a sense point of a sense line;

driving a word line and a serpentine bit line with first and second currents, respectively, the first and second currents selected to set first and second memory cells on the sense line with complementary values, the first and second memory cells associated with the word line, the serpentine bit line, and the sense line;

reading a second voltage at the sense point of the sense line;

determining the value from the first and second voltages; and

resetting the first and second memory cells to their original values.

8. The method of claim 7, wherein reading a first voltage at the sense point comprises:

driving the sense line with a current; and

reading a voltage at the sense point.

9. The method of claim 8, wherein determining the value comprises comparing the first and second voltages.

10. A method for storing data in first and second complementary cells of an array

of magneto-resistive memory cells, the method comprising:

driving a word line associated with the first and second cells with a first current; and

driving a serpentine bit line associated with the first and second cells with a second current such that the first and second cells, located on opposite sides of a sense point of a sense line, are set to opposite states to store the data.

11. The method of claim 10, wherein driving the word line with a first current comprises driving the word line with a current that passes the first cell in a first direction and passes the second, complementary cell in a second, substantially different direction.

12. The method of claim 10, wherein driving the serpentine bit line with a second current comprises driving the serpentine word line with a current that passes the first cell in a first direction and passes the second, complementary cell in a second, substantially opposite direction.

13. A memory array for a magneto-resistive memory device, the array comprising:
a plurality of memory cells disposed in rows and columns in the memory array;

wherein each memory cell in each row is paired with another memory cell in the same row such that the pair of memory cells are driven to first and second, different states by applying a single set of signals; and

a sense point for each row, the sense point located in the row at a point with one of the memory cells of each pair on one side of the sense point and the other memory cell of each pair located on the other side of the sense point.

14. The memory array of claim 13, and further comprising a plurality of word lines and a plurality of serpentine bit lines, the word lines and bit lines carrying the signals that drive the memory cells in a pair to opposite states.

15. A memory array for a magneto-resistive memory device, the array comprising:
means for storing a plurality of data bits as pairs of complementary values;
means for setting the pair of complementary values for a selected data bit in
the means for storing using the same signals to store each of the complementary
values in the pair of complementary values; and
means for reading a data bit from the means for storing using selected
complementary values in the means for storing.
16. The memory array of claim 15, wherein the means for storing comprises an
array of magneto-resistive memory cells, each row of the array including a plurality of
complementary pairs of memory cells.
17. The memory array of claim 15, wherein the means for storing comprises:
an array of memory cells disposed in a plurality of rows and columns;
a plurality of serpentine bit lines, the bit lines passing adjacent to each
memory cell in a row of the array;
a plurality of word lines, each word line passing adjacent to first and second
complementary memory cells in each row of the array.
18. The memory array of claim 15, wherein the means for reading comprises a
plurality of sense lines coupled to the means for storing for sensing the
complementary values.